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MAR 82 L A DUBITSKIY, Y I KUZ'MIN
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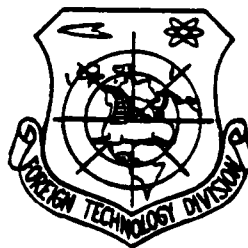
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ELECTRONIC COMMUTATOR

by

L.A. Dubitskiy and Yu.I. Kuz'min



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By: L.A. Dubitskiy and Yu.I. Kuz'min

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PREPARED BY:

TRANSLATION DIVISION
FOREIGN TECHNOLOGY DIVISION
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U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

| Block | Italic | Transliteration | Block | Italic | Transliteration |
|-------|------------|-----------------|-------|------------|-----------------|
| А а | <i>А а</i> | A, a | Р р | <i>Р р</i> | R, r |
| Б б | <i>Б б</i> | B, b | С с | <i>С с</i> | S, s |
| В в | <i>В в</i> | V, v | Т т | <i>Т т</i> | T, t |
| Г г | <i>Г г</i> | G, g | У у | <i>У у</i> | U, u |
| Д д | <i>Д д</i> | D, d | Ф ф | <i>Ф ф</i> | F, f |
| Е е | <i>Е е</i> | Ye, ye; E, e* | Х х | <i>Х х</i> | Kh, kh |
| Ж ж | <i>Ж ж</i> | Ch, ch | Ц ц | <i>Ц ц</i> | Ts, ts |
| З з | <i>З з</i> | Z, z | Ч ч | <i>Ч ч</i> | Ch, ch |
| И и | <i>И и</i> | I, i | Ш ш | <i>Ш ш</i> | Sh, sh |
| Я я | <i>Я я</i> | Y, y | Щ щ | <i>Щ щ</i> | Shch, shch |
| К к | <i>К к</i> | K, k | Ъ ъ | <i>Ъ ъ</i> | " |
| Л л | <i>Л л</i> | L, l | Ы ы | <i>Ы ы</i> | Y, y |
| М м | <i>М м</i> | M, m | Ь ь | <i>Ь ь</i> | ' |
| Н н | <i>Н н</i> | N, n | Э э | <i>Э э</i> | E, e |
| О о | <i>О о</i> | O, o | Ю ю | <i>Ю ю</i> | Yu, yu |
| П п | <i>П п</i> | P, p | Я я | <i>Я я</i> | Ya, ya |

*ye initially, after vowels, and after ъ, ы; e elsewhere.
When written as ё in Russian, transliterate as yë or ë.

RUSSIAN AND ENGLISH TRIGONOMETRIC FUNCTIONS

| Russian | English | Russian | English | Russian | English |
|---------|---------|---------|---------|----------|--------------------|
| sin | sin | sh | sinh | arc sh | sinh ⁻¹ |
| cos | cos | ch | cosh | arc ch | cosh ⁻¹ |
| tg | tan | th | tanh | arc th | tanh ⁻¹ |
| ctg | cot | cth | coth | arc cth | coth ⁻¹ |
| sec | sec | sch | sech | arc sch | sech ⁻¹ |
| cosec | csc | csch | csch | arc csch | csch ⁻¹ |

| Russian | English |
|---------|---------|
| rot | curl |
| lg | log |

ELECTRONIC COMMUTATOR

Authors of invention - L.A. Dubitskiy and Yu.I. Kuz'min

The invention refers to electronic-measuring technology, is designed for obtaining a sequence of pulses, shifted in time and space, from an arbitrary number of pulses of different duration, and can be used in multichannel measuring systems, in systems of remote signaling, and in counting technology.

Widely used at present are electronic commutating devices which are a combination of separate two-phase triggers joined by means of logic circuits or chains of triggers separated by delay circuits, and also commutating devices which consist of triggers joined by a general emitter resistance and crossover circuits. These devices have a very narrow frequency band of synchronization of timing frequency at the assigned values of timing capacitors and a low load capacity owing to the unsaturated operating mode of the transistors.

The purpose of the proposed invention is to construct an electronic commutator which contains a small number of active elements and possesses high reliability. This is achieved by the fact that introduced into the commutator is a forbidden circuit, to one input of which, through a differentiating circuit, is connected a source of the interrogation pulses and to the other input - a source of pulsed power feed, and its output is connected to the second input of each of the coincidence circuits.

Figure 1 depicts a block diagram of an electronic commutator the control of which is carried out by means of a single-cycle

commutation of the pulse feed voltage, and Fig. 2 shows the block diagram of an electronic commutator the control of which is carried out by means of two-cycle commutation of the pulsed feed voltage.

The electronic commutator given on Fig. 1 consists of n pulse-potential comparison circuits 1, n storage circuits (capacitors) 2, n single-transistor amplifier-limiters 3, the output of which (collector of the transistor) is connected with the control input of the pulse-potential comparison circuits, and the input (base of the transistor) is connected through the storage circuit with the output of the same comparison circuits. The pulsed input of the comparison circuits is connected to the output of the forbidden circuit 4, connected by the inhibiting input through the differential circuit 5 with the source 6 of interrogation pulses and by the pulsed input with source 7 of the pulsed feed voltage. The output of each amplifier-limiter is connected with the input of the subsequent amplifier-limiter through the crossover capacitor or diode-capacitor circuit 8 so that formed is a chain of series connected amplifier-limiters.

In the initial state the $n-1$ transistors are closed, and one is opened. In these states the transistors can be found as long as possible due to the use of the auxiliary pulsed feed voltage arriving at the pulsed input of the inhibited circuit. Realization of these states is achieved in the following way.

When the amplifier-limiter 3 is disengaged, i.e., the transistor is inhibited, the voltage from the output of the transistor inhibits the pulse-potential coincidence circuit, preventing the passage of the pulsed feed voltage to the storage circuit. With this mode, formed on the base of the transistor is the cutoff bias, owing to which the transistor can be turned off for an infinitely long time.

The turning on^{of} the amplifier-limiter, i.e., the cutoff of the transistor, leads to a change in the potential at the control input of the pulsed potential coincidence circuit 1. It is opened, and the pulsed feed voltage begins to proceed to the storage circuit 2, reproducing the cutoff bias on the base of the transistor. The cutoff bias is held practically constant due to the boost charge of the storage circuit accomplished continuously by the pulses of the appropriate polarity. The transistor₂ can thus be found in the opened

state for as long as possible.

The interrogation pulse coming from source 6 of the interrogation pulses is differentiated by circuit 5 and in the form of a half-wave goes to the inhibited circuit 4, inhibiting the feed to the pulse-potential coincidence circuits 1 of the pulse feed voltage.

The short-term turning off of source 7 of the pulsed feed voltage causes the turning off of the opened transistor. Formed on its collector is the corresponding differential (of voltage), which is fed through the crossover circuit to the base of the next transistor and cuts it off. And further, the transistor is held in the opened state by the pulsed feed voltage, which appears at the output of the inhibited circuit 4 upon completion of the action of the interrogation pulse on it. The arrival of the next interrogation pulse turns off the given transistor and turns on the next one, i.e., the advancement from one transistor to the other is carried out by means of commutation of the pulsed feed voltage. This commutation is single-cycle, since the movement is provided by pulses of the same interrogation sequence.

For the purpose of increasing the speed of response of the commutator, it is expedient to use two-cycle commutation of the pulsed feed voltage.

The electronic commutator in which the advancement of the pulse is accomplished by means of two-cycle commutation of pulsed feed voltage is given on Fig. 2. It consists of n pulse-potential coincidence circuits 1, n storage circuits 2, n single-transistor amplifier-limiters 3, the output of which is connected with the control input of the pulse-potential coincidence circuits, and the input of which is connected through the storage circuit with the output of the same circuits. The enumerated n connections are divided into two groups, even and odd, with $n/2$ connections in a group. Each connection is connected by pulsed inputs of the pulse-potential coincidence circuits to the output of the corresponding inhibited circuits 9 and 10, which are connected by the inhibiting inputs with outputs of the two-cycle source of interrogation pulses 11, for example, a trigger with a counting start, and by pulsed inputs - with source 7 of the pulsed feed voltage. The output of each amplifier-

-limiter is connected to the input of the next amplifier-limiter through the crossover circuit 8 so that formed is a small chain of series connected amplifier-limiters with even and odd numbers.

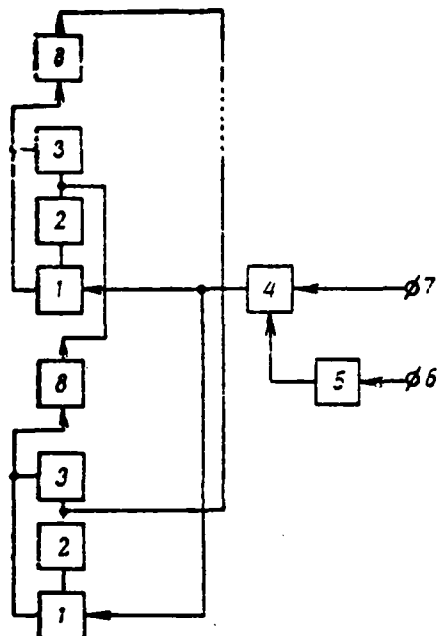


Fig. 1.

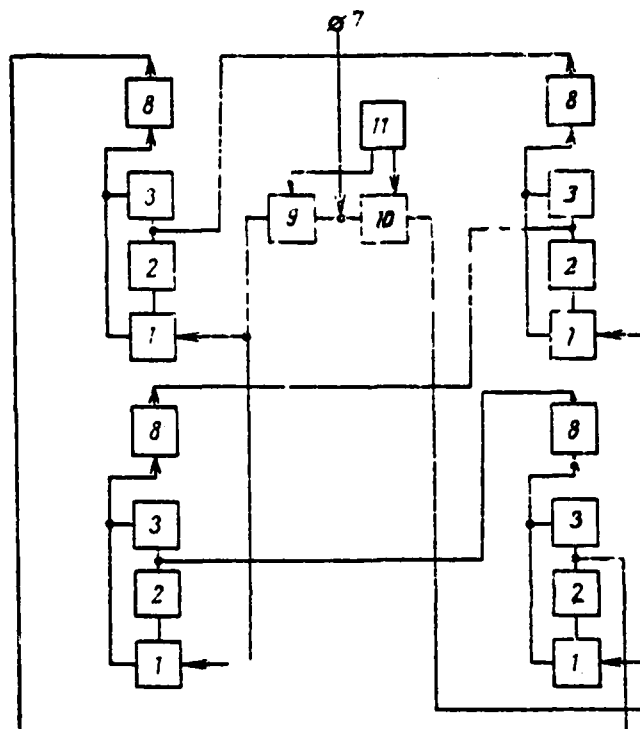


Fig. 2.

This electronic commutator operates in the following way.

In the initial state $n-1$ transistors are closed, and one is opened. The interrogation sequences taken from arms of the two-cycle source 6 of the interrogation pulses are sequences of pulses having the phase shift π . These sequences proceed to the inhibiting inputs of the inhibiting circuits, thus ensuring the commutation of the pulsed feed voltages on the buses connecting the pulsed inputs of the pulse-potential coincidence circuits of the even and odd groups with the phase shift π . This means that at any moment of time there is a pulsed feed voltage on one of the buses, and on the other it is absent.

Thus the transistor opened in the initial state is closed with removal from the bus, to which it is connected, of the pulsed feed

voltage. Formed on its collector is a voltage differential, which is fed through the crossover circuit to the base of the next transistor and cuts it off. Since each successive transistor is connected to the bus, the feed of which is carried out in an opposite phase to the preceding one, then, consequently, the triggering of the next transistor coincides in time with the appearance of the pulsed feed voltage, and the transistor remains turned on.

Thus the arrival of each following interrogation pulse causes commutation of the pulsed feed voltage on the buses and, correspondingly, the advancement from the preceding transistor to the next one. Such commutation is two-cycle, since the advancement is ensured by two sequences having a phase shift with respect to each other equal to π .

As was noted, the two-cycle commutation makes it possible to ensure the feed of each of the buses, which joins the pulsed inputs of the pulse-potential coincidence circuits of the even and odd groups out of phase. This means that the pulsed feed voltage is not fed to each disengaging transistor during a duration equal to 1/2 of the repetition interval of the interrogation pulses. Thus, unlike the commutators constructed according to the design with a single-cycle commutation of the pulse feed voltage, the time taken for recovery of capacitors of the connection amplifier-limiter-storage circuit-pulse-potential coincidence circuit is considerably increased, which leads, in turn, to an increase in the speed of response of the commutators with two-cycle commutation, although it requires a certain increase in equipment.

Thus from the operation of circuits of electronic commutators, it is evident that they are quite simple, and transistors required for their construction are twice less than those in the known circuits. And this, in turn, is indicative of the higher reliability and lower cost of the proposed circuits.

Claim of the invention

An electronic commutator consisting of n series connected groups each containing a pulse-potential coincidence circuit, a storage capacitor, and amplifier-limiter, the output of which is connected to

one input of the coincidence circuit, which is different in that for the purpose of reducing the number of active elements and increasing the reliability, introduced into the commutator is an inhibiting circuit, to one input of which connected through a differentiating circuit is a source of interrogation pulses, and to the other input there is connected the source of the pulsed feed, and its output is connected to the second input of each of the coincidence circuits.

5-8